

FIGURE 1

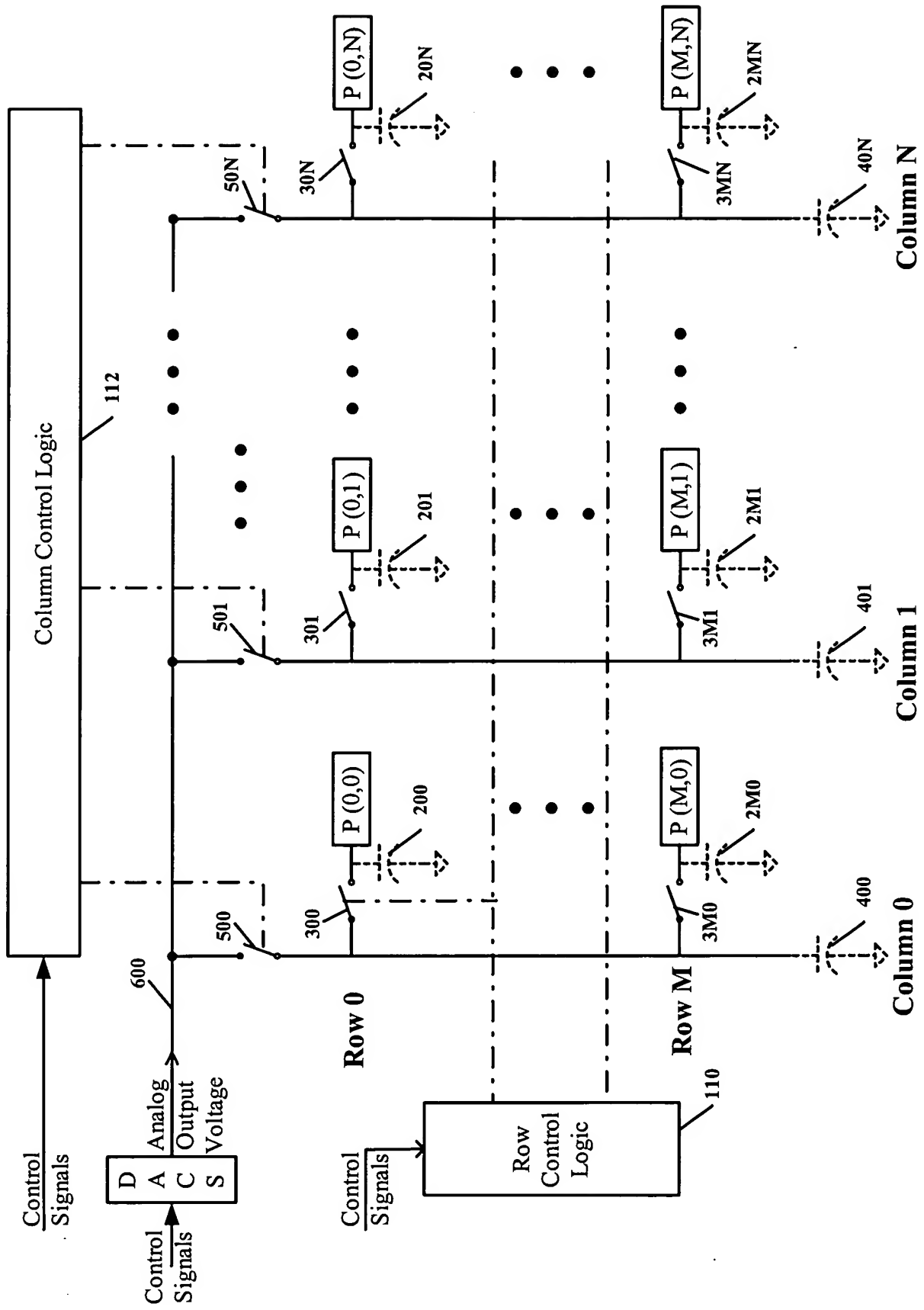


FIGURE 2

FIG. 3 is a schematic diagram of a memory array structure in accordance with the present invention. The array is organized into rows and columns. Each row is connected to a row control line (RCL) and each column is connected to a column control line (CCL). The array is divided into two main sections: a top section and a bottom section. The top section contains a row of memory cells (P(0,0) to P(0,N)) and the bottom section contains a row of memory cells (P(M,0) to P(M,N)). Each memory cell is connected to a row control line and a column control line. The row control lines are connected to a row control logic block (110) and the column control lines are connected to a column control logic block (112). The row control logic block (110) receives control signals (D, A, C, S) and provides control signals to the row control lines. The column control logic block (112) receives control signals and provides control signals to the column control lines. The array is also connected to a fixed voltage source (602) and an analog output voltage source (600). The array is controlled by a 'Close Aux SW' signal (600) and a 'Control Signals' input (D, A, C, S). The array is organized into rows (Row 0 to Row M) and columns (Column 0 to Column N). Each row is connected to a row control line (RCL) and each column is connected to a column control line (CCL). The array is divided into two main sections: a top section and a bottom section. The top section contains a row of memory cells (P(0,0) to P(0,N)) and the bottom section contains a row of memory cells (P(M,0) to P(M,N)). Each memory cell is connected to a row control line and a column control line. The row control lines are connected to a row control logic block (110) and the column control lines are connected to a column control logic block (112). The row control logic block (110) receives control signals (D, A, C, S) and provides control signals to the row control lines. The column control logic block (112) receives control signals and provides control signals to the column control lines. The array is also connected to a fixed voltage source (602) and an analog output voltage source (600). The array is controlled by a 'Close Aux SW' signal (600) and a 'Control Signals' input (D, A, C, S). The array is organized into rows (Row 0 to Row M) and columns (Column 0 to Column N). Each row is connected to a row control line (RCL) and each column is connected to a column control line (CCL). The array is divided into two main sections: a top section and a bottom section. The top section contains a row of memory cells (P(0,0) to P(0,N)) and the bottom section contains a row of memory cells (P(M,0) to P(M,N)). Each memory cell is connected to a row control line and a column control line. The row control lines are connected to a row control logic block (110) and the column control lines are connected to a column control logic block (112). The row control logic block (110) receives control signals (D, A, C, S) and provides control signals to the row control lines. The column control logic block (112) receives control signals and provides control signals to the column control lines. The array is also connected to a fixed voltage source (602) and an analog output voltage source (600). The array is controlled by a 'Close Aux SW' signal (600) and a 'Control Signals' input (D, A, C, S).

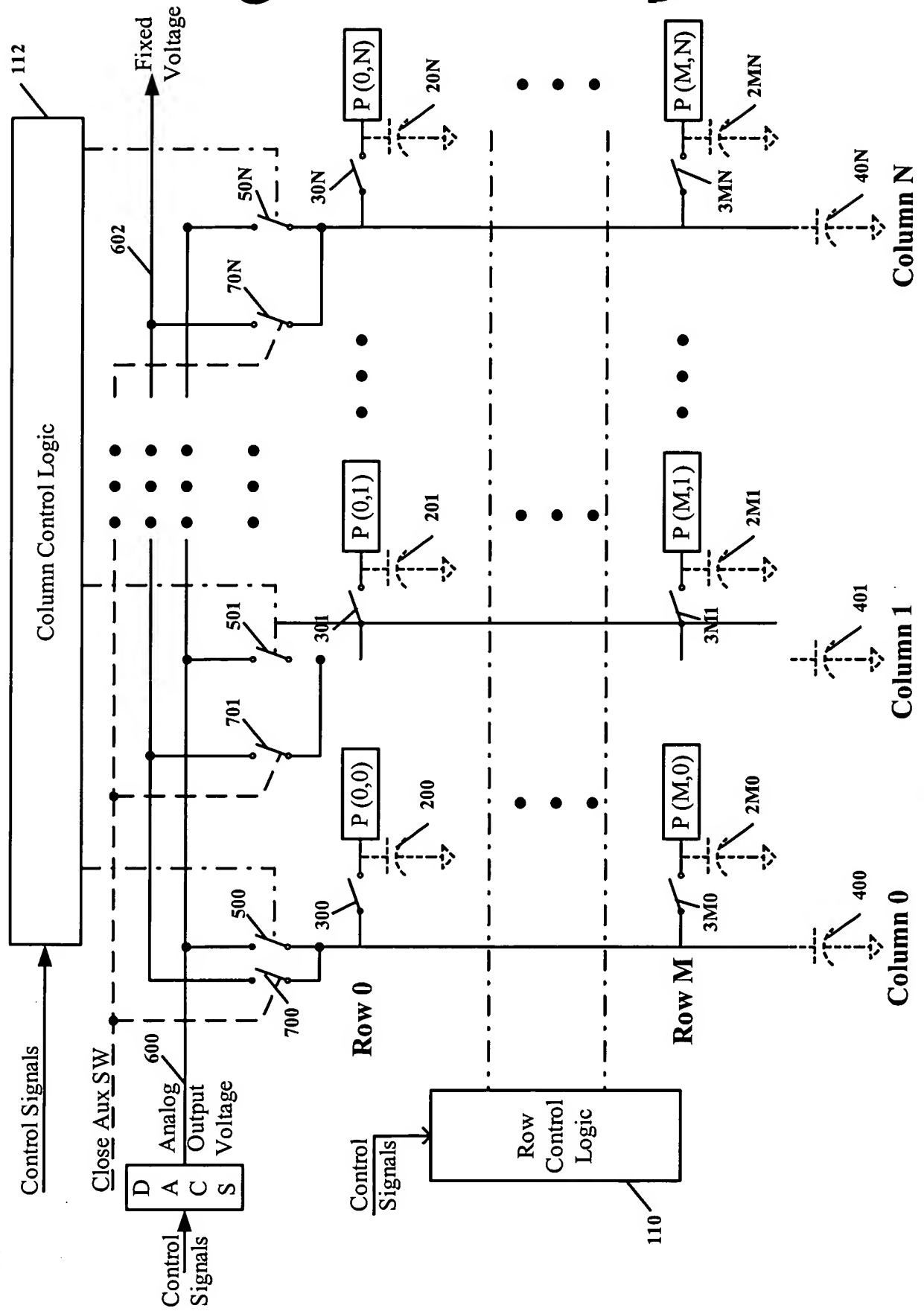


FIGURE 3

FIG. 4 is a schematic diagram of a crossbar array circuit. The circuit includes a control logic block 112, a row control logic block 110, and a crossbar array of switches. The switches are controlled by control signals and are connected to a pin 112. The switches are arranged in a grid of rows and columns. The rows are labeled Row 0, Row M, and Row N. The columns are labeled Column 0, Column 1, and Column N. The switches are labeled with their row and column coordinates, such as P(0,0), P(0,1), P(0,N), P(M,0), P(M,1), P(M,N), and P(N,0), P(N,1), P(N,N). The switches are controlled by control signals and are connected to a pin 112. The switches are arranged in a grid of rows and columns. The rows are labeled Row 0, Row M, and Row N. The columns are labeled Column 0, Column 1, and Column N. The switches are labeled with their row and column coordinates, such as P(0,0), P(0,1), P(0,N), P(M,0), P(M,1), P(M,N), and P(N,0), P(N,1), P(N,N). The switches are controlled by control signals and are connected to a pin 112.

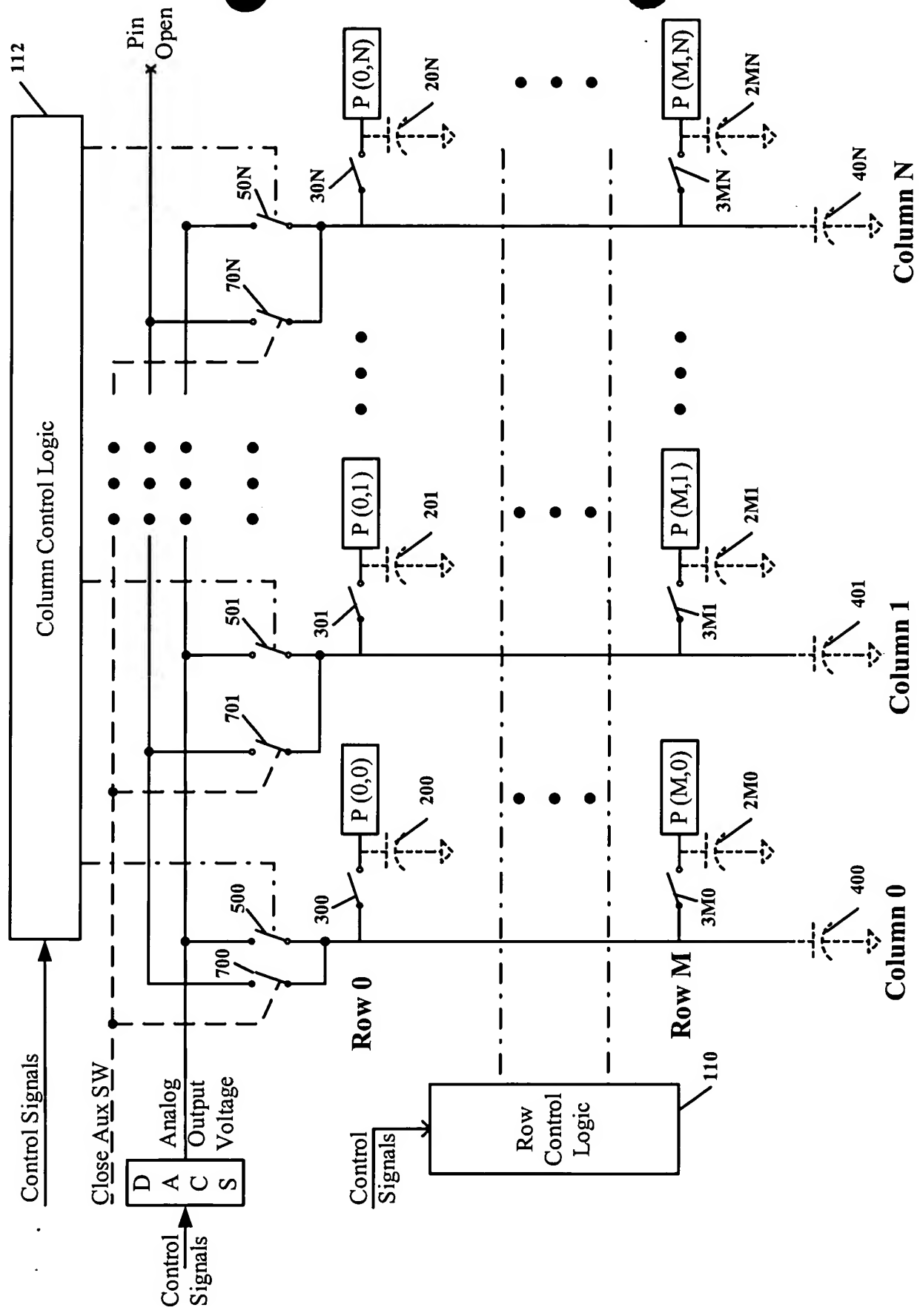


FIGURE 4

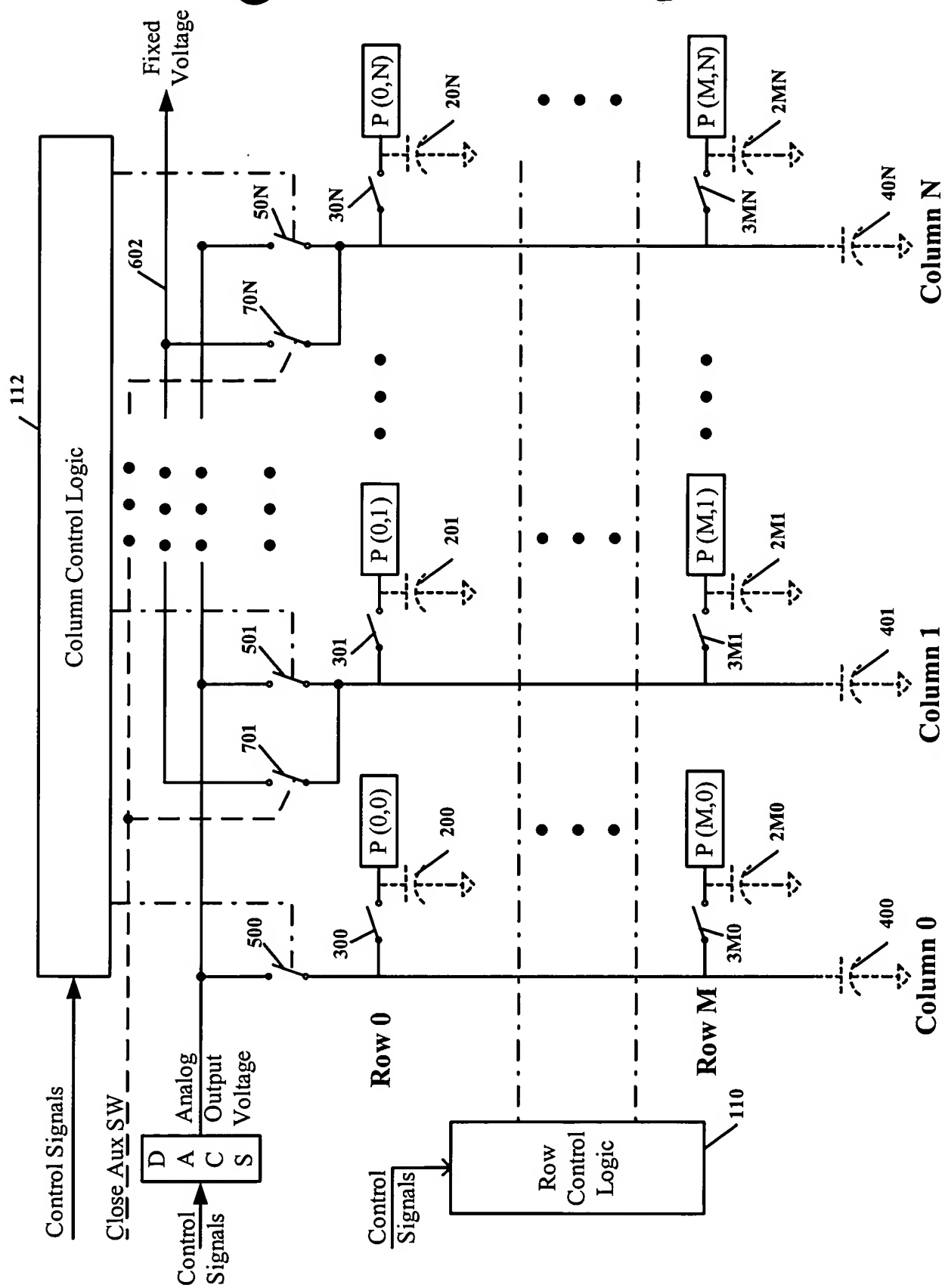


FIGURE 5

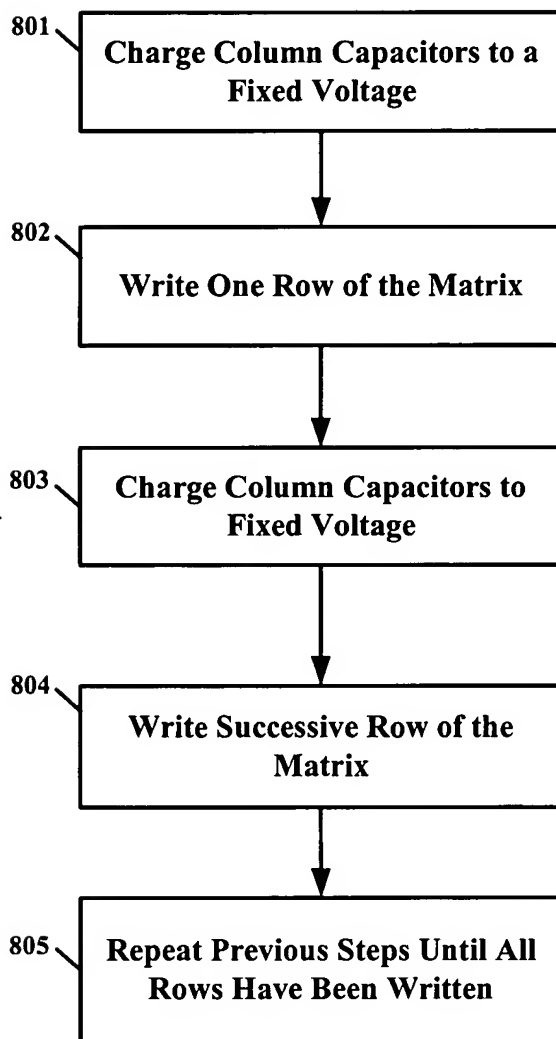


FIGURE 6

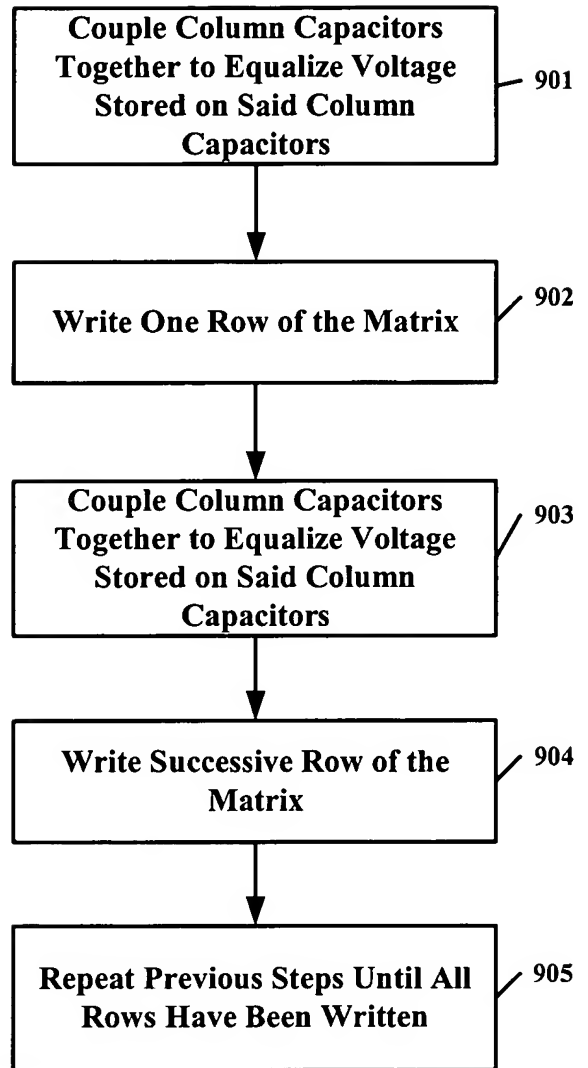


FIGURE 7

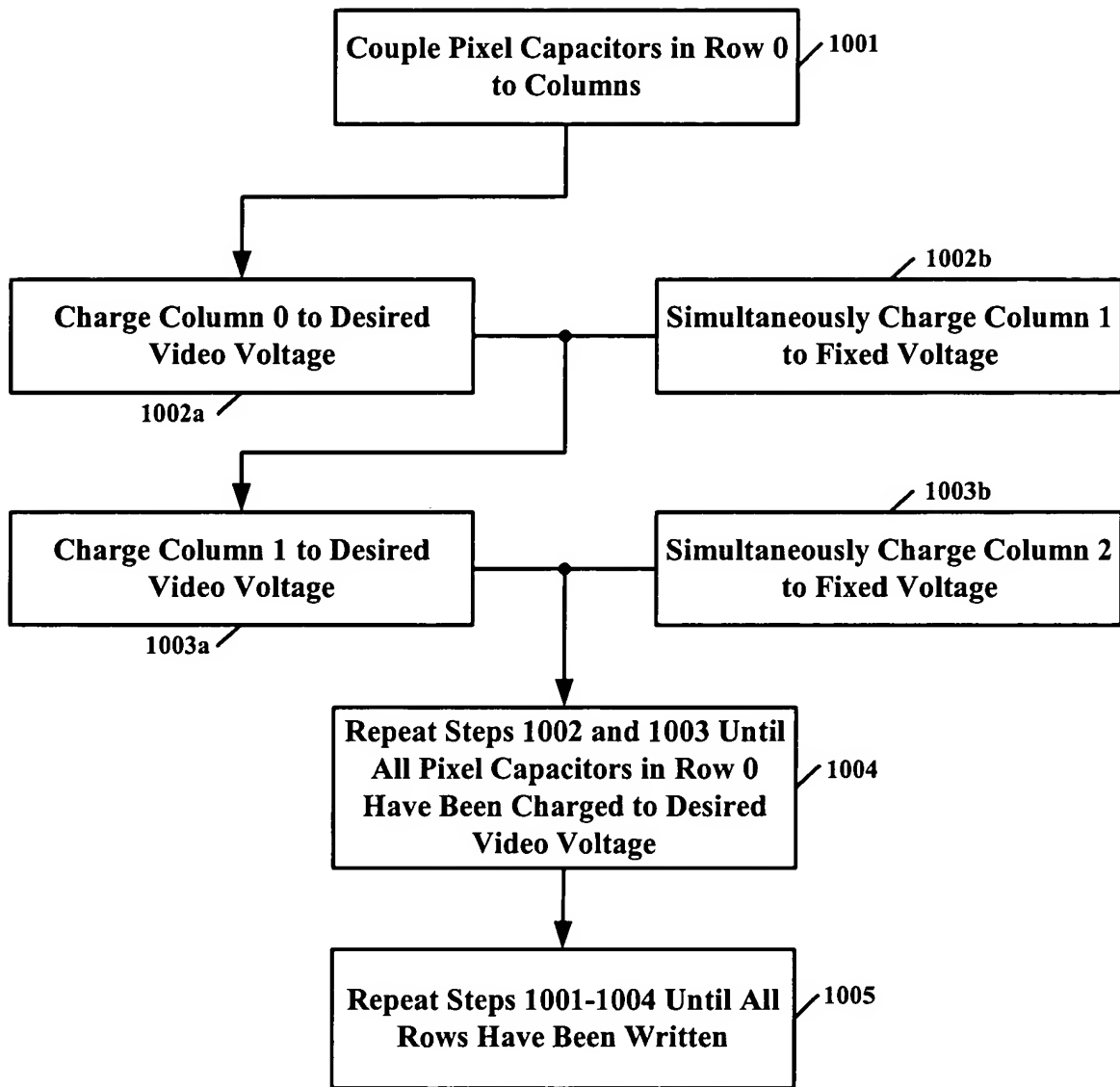


FIGURE 8